

Remarks

Applicant respectfully requests reconsideration of the rejection of the claims in view of the remarks set forth below. Claims 1-8 and 17-20 remain in the application. Claims 9-16 were previously canceled. Claims 1-8 and 17-19 were previously presented. Claim 20 remains unchanged.

35 U.S.C. §103

Claims 1-8 and 17-20 stand rejected under 35 U.S.C. 103 (a) as being unpatentable over Van de Kerkhof (US 5,995,493) in view of Ishizu (US 5,757,862). Under U.S.C. § 103, the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to be obvious in light of the teachings of the references (MPEP § 706.02(j)).

Claim 1 recites a “digital radio frequency (RF) circuit that creates a signal in a desired range in a frequency spectrum, comprising... circuitry that produces a first sample data modulated signal having a first frequency and a first sample data clock rate... an up-sampler modulator that receives the first sample data modulated signal and produces a second sample data modulated signal having a second frequency and a second sample data clock rate... and circuitry that receives the first sample data modulated signal and the second sample data modulated signal and *delivers one of the first sample data modulated signal and the second sample data modulated signal for further processing* depending on which sample data modulated signal exhibits desirable characteristics for a given operating environment.” (Emphasis added).

The “circuitry that receives the first sample data modulated signal and the second sample data modulated signal and *delivers one of the first sample data modulated signal and the second sample data modulated signal for further processing* depending on which sample data modulated signal exhibits desirable characteristics for a given operating environment” element of claim 1 is an important aspect of Applicant’s claimed invention. As discussed on page 6, lines 21-29 of Applicant’s application:

The use of two clock modes in accordance with the present invention may result in a number of advantages. One advantage is that power consumption savings may be obtained by using the lower clock rate circuitry without the need to replicate circuitry. Another advantage is that EMI emissions are different for the two modes of operation. This gives system designers flexibility to choose whichever mode of operation is most compatible with a desired EMI profile. A third advantage is that dynamic range (analog resolution) of the inchannel IF signal for the low clock rate mode is the same as the dynamic range of the inchannel IF signal for the high clock rate mode, even though the signal levels are different.

In other words, the present invention permits a system designer to have flexibility in adjusting the characteristics (e.g., power consumption, EMI emission profile, etc.) of a digital RF circuit when the RF circuit contains the “circuitry that receives the first sample data modulated signal and the second sample data modulated signal *and delivers one of the first sample data modulated signal and the second sample data modulated signal for further processing depending on which sample data modulated signal exhibits desirable characteristics for a given operating environment*” (emphasis added) element of claim 1.

Van de Kerkhof appears to be directed towards providing an extension to the format of a transmission signal such that a digital signal is transmitted having both a lowpass filtered and downsampled component having a sampling frequency f_{s2} and a high frequency component having a sampling frequency f_{s1} . (Col. 1, lines 24-29; col. 4, lines 27-30, 40-42, and 62-67; and FIG. 1). Using the transmission signal of Van de Kerkhof, legacy receivers recover the digital signal by only retrieving and processing the lowpass filtered and downsampled component of the transmitted signal (FIG 3; col. 2, lines 20-25; col. 3, line 66 to col. 6, line 7) while Van de Kerkhof-based receivers recover the digital signal by retrieving and processing both the lowpass filtered and downsampled component and the high frequency component of the transmitted signal (Fig. 2; col. 5, lines 29-65). As a result, Van de Kerkhof appears to teach the transmitting or further processing of a signal having both a first signal component having a sampling frequency f_{s1} and a second downsampled signal component having sampling frequency f_{s2} . Indeed, as noted on page 3 of the July 10, 2008 office action, “Van de Kerkhof however, does not explicitly disclose circuitry that receives the first and second modulated signal delivers one of the modulated signal depending on which sample data modulated signal exhibits desirable characteristics for a given operating environment.”

The office action proposes that Ishizu discloses the element missing in Van de Kerkhof. Applicant respectfully disagrees. As shown in Figs. 2A and 2B and discussed in column 7, lines 28-32, the Ishizu selector 24 receives signals $R(nT)$ and $D(nT)$ and outputs signals I_c and Q_c . As explicitly shown in Fig. 2B, I_c and Q_c are either $R(t)$ and $D(t)$, $-D(t)$ and $R(t)$, $-R(t)$ and $-D(t)$, or $D(t)$ and $-R(t)$. Therefore, selector 24 always outputs both $R(t)$ and $D(t)$ and never outputs only one of $R(t)$ or $D(t)$. In contrast to Ishizu, claim 1 recites, inter alia, “circuitry that receives the first sample data modulated signal and the second sample data modulated signal *and delivers one of the first sample data modulated signal and the second sample data modulated signal for further processing depending on which sample data modulated signal exhibits desirable characteristics for a given operating environment.*”

As a result, Applicants respectfully propose that the combination of Van de Kerkhof and Ishizu, fail to suggest the “circuitry that receives the first sample data modulated signal and the second sample data modulated signal *and delivers one of the first sample data modulated signal and the second sample data modulated signal for further processing depending on which sample data modulated signal exhibits desirable characteristics for a given operating environment*” element of claim 1. Therefore, it is respectfully proposed that the rejection of claim 1 under 35 U.S.C. § 103(a) is overcome in accordance with the above remarks and notice to that effect is earnestly solicited.

Dependent claims 2-8 being dependent on and further limiting independent claim 1, should be allowable for that reason, as well as for the additional recitations that they contain. Applicant respectfully requests reconsideration of the rejection of the claims in view of the above remarks.

Independent claim 17 contains elements similar to independent claim 1 and should be allowable for the reasons discussed above. Therefore, it is respectfully proposed that the rejection for obviousness is overcome.

Dependent claims 18-20 being dependent on and further limiting independent claim 17, should be allowable for that reason, as well as for the additional recitations that they contain. Applicant respectfully requests reconsideration of the rejection of the claims in view of the above remarks.

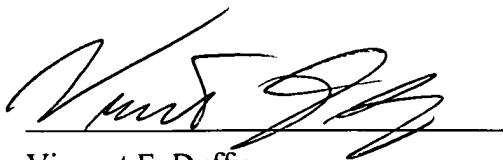
Having fully addressed the Examiner's rejections it is believed that, in view of the preceding remarks, this application stands in condition for allowance. Accordingly then, reconsideration and allowance are respectfully solicited. If, however, the Examiner is of the opinion that such action cannot be taken, the Examiner is invited to contact the Applicants' attorney at (818) 260-3727, so that a mutually convenient date and time for a telephonic interview may be scheduled.

Ser. No. 10/572,695

PU030265

No fees, other than those discussed above, are believed due. However, if a fee is due, please charge the additional fee to Deposit Account 07-0832.

Respectfully submitted,



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Patent Operations

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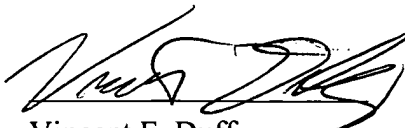
Princeton, New Jersey 08543-5312

January 9, 2009

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I hereby certify that this amendment is being deposited with the United States Postal Service as First Class Mail, postage prepaid, in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on:

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Vincent E. Duffy

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